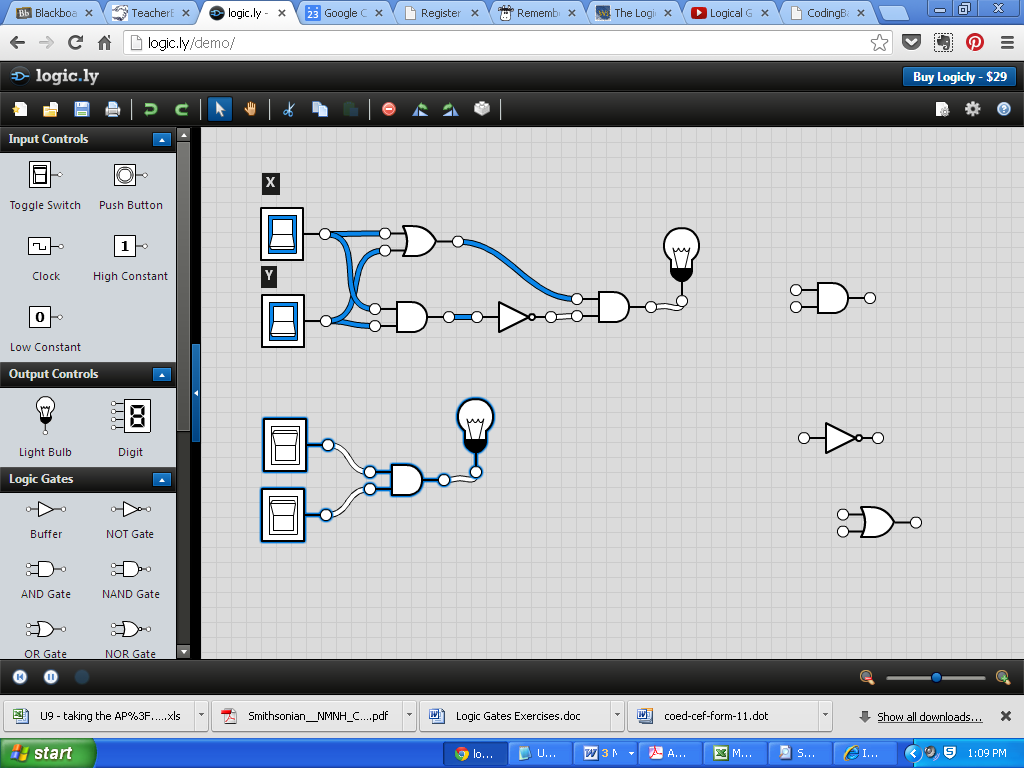
**Student Activity Guide: Circuits** Name \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

Unit 3 Lesson 12

**Directions**

For each table, draw a logic gate that will yield the indicated result. Use the tools at <http://logic.ly/demo/> to test your solutions.

**Example:**



|  |  |  |
| --- | --- | --- |
| **Input** | | **Output** |
| **X** | **Y** |  |
| 1 | 1 | 1 |
| 1 | 0 | 0 |
| 0 | 1 | 0 |
| 0 | 0 | 0 |

**Problem 1:**

|  |  |  |
| --- | --- | --- |
| **Input** | | **Output** |
| **X** | **Y** |  |
| 1 | 1 | 0 |
| 1 | 0 | 1 |
| 0 | 1 | 1 |
| 0 | 0 | 1 |

**Problem 2:**

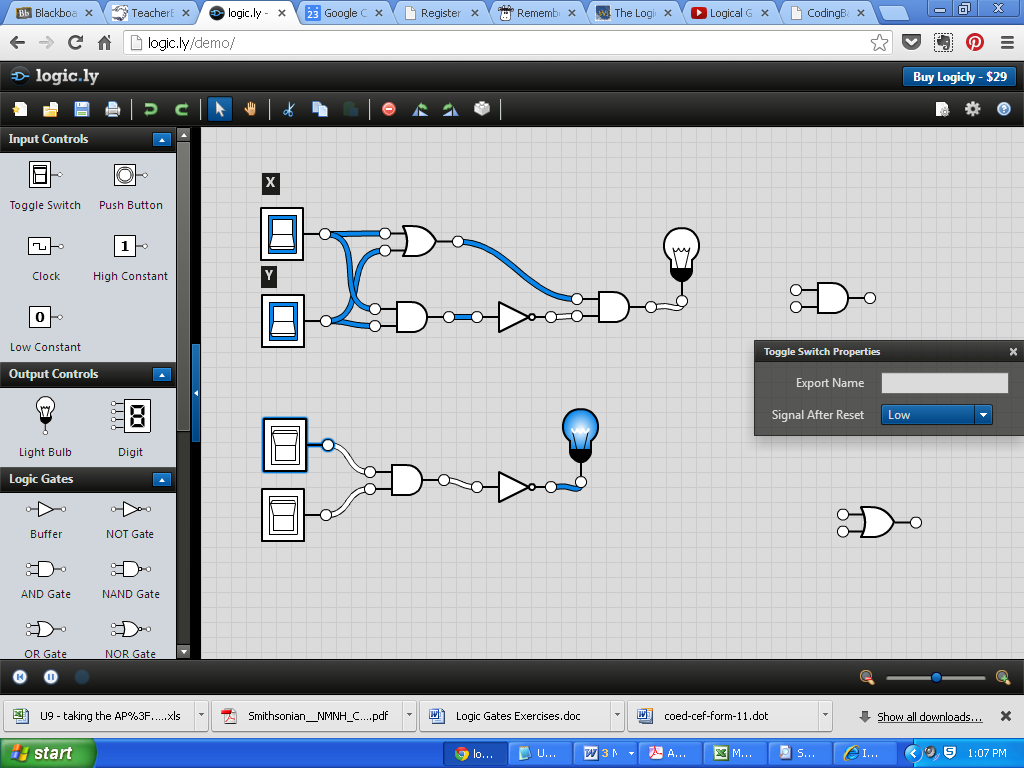
|  |  |  |
| --- | --- | --- |
| **Input** | | **Output** |
| **X** | **Y** |  |
| 1 | 1 | 0 |
| 1 | 0 | 1 |
| 0 | 1 | 1 |
| 0 | 0 | 0 |

**Problem 3:**

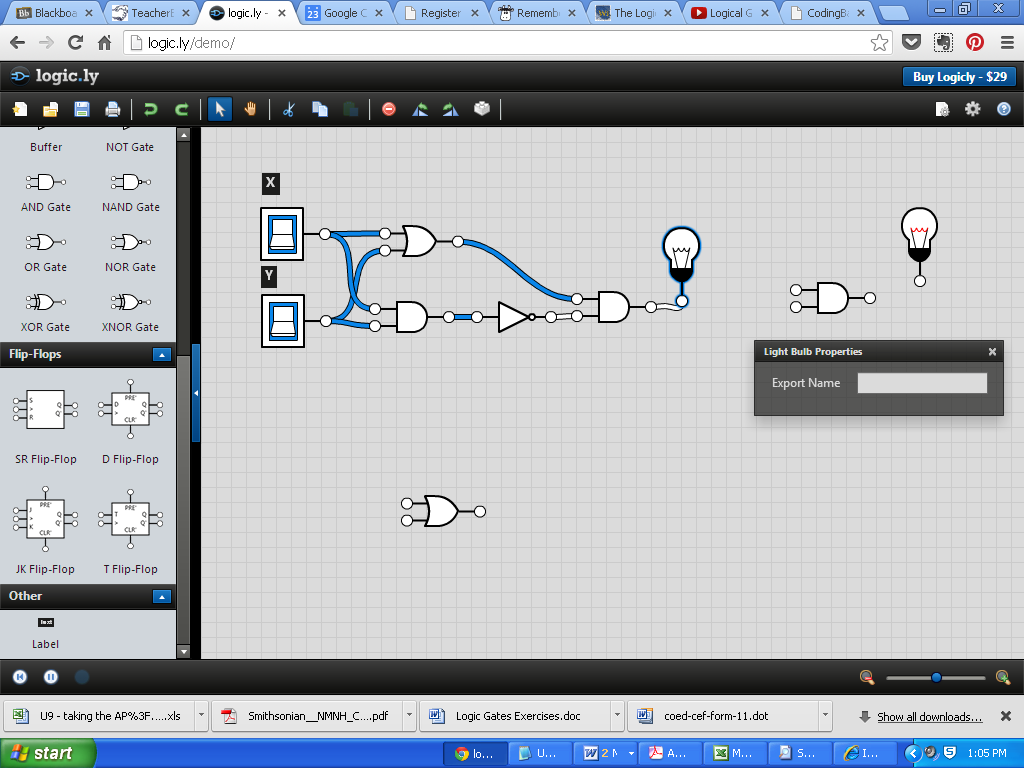
|  |  |  |  |
| --- | --- | --- | --- |
| **Input** | | | **Output** |
| **X** | **Y** | **Z** |  |
| 1 | 1 | 1 | 1 |
| 1 | 1 | 0 | 1 |
| 1 | 0 | 1 | 1 |
| 1 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 0 |
| 0 | 0 | 1 | 0 |
| 0 | 0 | 0 | 0 |

**ANSWERS**

Problem 1:



Problem 2: Notice that this is nesting X != Y (how if’s work)



Problem 3:

